**SkyFlash EC Project: Architecture for a 1Mbit S-Flash for Space Applications**

A. Arbat¹, C. Calligaro¹, V. Dayan², E. Pikhay² and Y. Roizin²

¹ RedCat Devices, Via Valsolda 21, Milano, Italy  
² Tower Semiconductors, Migdal Haemek, Israel  

*Email: a.arbat@redcatdevices.it*

---

**MOTIVATION AND RADIATION EFFECTS**

Radiation effects are divided into:

Cumulative effects:
- Total Ionizing Dose (TID)
- Displacement Damage Dose (DDD)

Single event effects, hard errors:
- Single Event Latch-up (SEL)
- Single Event Gate Rupture (SEGR)

Single event effects, soft errors:
- Single Event Upset (SEU)
- Single Event Transient (SET)
- Multiple Bit Upset (MBU)
- Single Event Functional Interrupt (SEFI)

---

**S-FLASH MEMORY CELL**

*Working principle:* modification of the threshold voltage of a MOS transistor by trapping charge in a storage layers. In the S-Flash cell the storage media are the nitride spacers (high number of traps) instead of the typical ONO structure [1]. The implantation profiles have been optimized to have a high efficiency of hot carrier generation (PI) by adding only 1 additional mask to the standard CMOS process. The cell size is 1.12µm*1.12µm.

*PROGRAM/ERASE METHOD*

Programming and erasing of the cells are based on hot carrier mechanism (CHE) and hot holes generated by band-to-band (BTB) tunneling. The injection of charge in the nitride produces a shift on the threshold voltage. The programming is done from the drain side with voltages of 5-6V using 3.3V transistors.

*READ METHOD*

Each bit is represented with different Vth values and the distance between them is the operation window. Reading is done on the reverse direction of programming (source), allowing to separate high voltage circuitry from the reading stage.

---

**MEMORY ARCHITECTURE RADIATION ENHANCEMENT**

**A) DIFFERENTIAL CELL APPROACH**

| Problem: | Vth shift of the S-Flash cells due to the loss of charge when irradiated. |
| Solution: | Instead of using a reference cell for reading, two cells are used to store a single bit, one containing the bit and one the negated bit. |

---

**B) AVOID SEE IN THE DIFFERENTIAL CELL**

| Problem: | The small dimensions of the S-flash cell can produce multiple cells affected due to a SEE [2]. |
| Solution: | The two cells corresponding to the single bit are placed in two independent arrays. |
| | The minimum distance between the two cells of the bit is 70µm. |
| | Specula distribution compensates the capacitive load when reading. |

---

**C) LIMITATION OF THE ERASE DISTURB AT PROGRAMMING**

| Problem: | Erase disturb at programming, when programming a cell the neighbor cells in the same bit-line at exposed to weak erasing conditions. |
| Solution: | The maximum number of cells sharing a bit lines should not exceed 128. Each bit contains two arrays of 128kcells divided in two arrays of 128 rows and 512 columns. This limitation is related to programming but not to reading. |
| | The high voltage stages are duplicated and placed on the external sides, while the reading electronics is unique and placed in the middle of the array. |

---

**BIBLIOGRAPHY**